AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Previously presented) A method for forming a spacer, comprising:

depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

applying a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area, the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

2. (Previously presented) The method of claim 1 wherein the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines.

3-5. (Cancelled).

6. (Currently amended) ~~The process of claim 5,~~ A process for fabricating a non-volatile memory device comprising:

providing a substrate having a core area, a periphery area, and at least two adjacent polysilicon lines in each of the core area and the periphery area;

depositing a first oxide layer over the adjacent polysilicon lines, ~~wherein~~ the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

depositing a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area.

7-14. (Cancelled).

15. (New) The process of claim 6, further comprising performing a second spacer etch over the core area.

16. (New) The process of claim 6, the implanting of an area occurs after the performing of the first spacer etch.

17. (New) The process of claim 6, further comprising implanting an area located between at least two polysilicon lines in the periphery area.

18. (New) The process of claim 17, the implanting of an area located between at least two polysilicon lines in the periphery area occurs after the performing of the first spacer etch.

19. (New) The process of claim 17, the implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

20. (New) The process of claim 6, the substrate is a silicon wafer.

21. (New) The process of claim 6, the depositing of the first oxide layer comprising passing nitrogen dioxide gas over the substrate.

22. (New) The process of claim 6, further comprising depositing a nitride layer between the first oxide layer and the second oxide layer.

23. (New) The process of claim 22, the depositing of the nitride layer comprising passing a gas composed of at least silicon, hydrogen and ammonia.

24. (New) The process of claim 6, the depositing of the first oxide layer partially fills an interstitial gap between adjacent polysilicon lines.

25. (New) The process of claim 6, the core area retaining an amount of the second oxide between adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

26. (New) The method of claim 1, further comprising implanting an area located between at least two adjacent polysilicon lines in the periphery area.

27. (New) The method of claim 26, the implanting of the area located between at least two polysilicon lines in the periphery area occurring subsequent to performing the first spacer etch.

28. (New) The method of claim 1, the implanting of the area located between at least two adjacent polysilicon lines occurs after application of the second spacer etch.

29. (New) The method of claim 1, prior to performing the second spacer etch depositing resist over the periphery area.

30. (New) The method of claim 1, prior to implanting an area between at least two adjacent polysilicon lines masking the core area and the periphery area.